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REMARKS/ARGUMENTS

1.) Claim Amendments

The Applicant has amended claims 1, 2, 5-9, 11, 20, 25-26, 30-31, 34-38, 45-46, 48-49, 51-53, and 55. Claim 39 has been canceled without prejudice. Accordingly, claims 1-38 and 40-55 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

The claims have been amended in response to the Examiner's objections and §112 rejections. Consequently, they do not raise new issues that would require a further search or substantial consideration by the Examiner.

2.) Examiner Objections

The Examiner objected to claims 6, 11, 25 and 46 due to informalities. The Applicants have amended the claims to correct the informalities. The Examiner's consideration of the amended claims is respectfully requested.

3.) Claim Rejections – 35 U.S.C. § 112

The Examiner rejected claims 1-55 under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Applicant thanks the Examiner for his thorough review of the claims and has amended the claims to address this rejection. The Examiner's consideration of the amended claims is respectfully requested.

Specifically, the term "part entities of the load module" has been replaced with the term "parts of the load module" in claims 1, 30, 48, 52 and the associated child claims.

In claim 6, the term "a first type of load data" has been deleted. It is now clear that the term "both types of data" refers to variable/record data or instruction data.

In claim 25, the term "later occasion" has been replaced with the term "during steady-state operation of the system.

Claim 39 has been canceled without prejudice. So, the Examiner's rejection with respect to this claim is deemed moot.

Claim 46 has been modified to state that the packing occurs periodically and/or after large reallocations of data.

Claim 20 has been amended to depend from claim 18 and claim 26 has been amended to depend from claim 25.

4.) Claim Rejections – 35 U.S.C. § 102(e)

The Examiner rejected claims 1-3, 5-8, 10, 14, 21-28, 30-32, 34-37 and 43-47 under 35 U.S.C. § 102(e) as being anticipated by Spear, et al. (US 6,003.115). The Applicant respectfully traverses this rejection.

Spear appears to disclose a disk cache method in a system having a processor and memories arranged in a memory hierarchy. The most frequently used data is stored in fast memory, a so-called processor cache, while less frequently used data is stored in main memory. Data that is rarely used is stored on a disk. A portion of main memory constitutes a disk cache. Data stored on disk that is being most frequently used is stored in said portion of main memory as well. The disk cache is operated upon by means of software control. Data is arranged in blocks, which blocks are handled according to a "Least Frequently Used" (LRU) algorithm. An end-user application never accesses said blocks directly. Rather, the blocks that have end-user application data for an application are copied to a different portion of the main memory before being used by the end-user application. The LRU algorithm performs disk access profiling for determining the data to be stored in the disk cache.

Therefore, Spear appears to teach a preloading of a software-controlled disc cache. As one skilled in the art would recognize, disc caches reside in main memory (i.e. in RAM) of a computer, but they are accessed block wise (instead of random access) in the same way as a disc. The contents of a disc cache are never directly addressed by an application. The contents of a disc cache are instead copied to the user/application area in the memory by the operating system before it is used by the application program.

The specification of Spear also describes a conventional computer having a standard (e.g. hardware controlled) cache to speed up the execution in the processor. The Applicant believes that the hardware cache is not relevant to the disc cache nor the claims in the Spear patent. The mention of hardware cache just happens to be in the description since it is a standard part of most modern computers. For example, the examiner states that Spear teaches the use of "a second RAM" and refers to col 2, lines 25-28. However, these lines refer to the processor cache. This cache is not used in the software-controlled disc cache of Spear, but is only briefly shown in a general description of a computer.

In contrast, the claimed invention is directed towards processor cache handling where caches are based on run-time program performance and operating system knowledge. The processor cache is distinct from disc cache. Furthermore, data is stored in the processor cache in accordance with program-performance information gathered through program execution profiling, and in accordance with execution-priority information gathered from an operating system. In the claimed invention, the memory cache is random assessable – as opposed to block accessible (as would be the case with disc cache). Consequently, the current invention does not use an LRU algorithm for handling the processor cache. Neither are end-user programs subjected to disk access profiling for the purpose of gathering information on program performance – as would be the case with disc cache.

For instance, claim 1 states:

> 1. A processor system comprising:
> a processor,
> a first memory, *being of a random access memory type*,
> a second memory, *being of a random access memory type*,
> memory allocation means for allocation of data of a load module of said second memory to said first memory, said load module comprising:
> variable/record data and/or instruction data,
> an execution profiling section for providing execution data concerning behavior of programs executed in the processor system, continuously or intermittently, *whereby the operation of said means for memory allocation is software run-time updated based on said execution data*, said execution profiling section in turn comprising at least one means for measuring the performance characteristics of parts of said load module,

whereby said memory allocation means is arranged for allocation of selected parts of said load module to said first memory.

Spear, in contrast, does not use two memories of a random access memory type. Furthermore, Spear does not update memory allocation by run-time software based on factors, such as execution data.

Because Spear does not teach all of the claim elements, the withdrawal of the 102 rejection is respectfully requested. As the examiner is aware, to sustain a 102 rejection, ALL elements of the claim must be taught by the cited art. As the Federal Circuit held:

> Under 35 U.S.C. §102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. . . . In addition, the *prior art reference must be enabling*, thus placing the allegedly disclosed matter in the possession of the public. *Akzo N.V. v. United States Int'l Trade Comm'n*, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), *cert. denied*, 482 U.S. 909 (1987) (Emphasis Added)

Thus, a 102 rejection is not appropriate in this situation because all the elements of claim 1 are simply not taught by Spear.

Claim 30 is allowable for the same reasons that claim 1 is allowable. Claims 2-3, 5-8, 10, 14, 21-28, 31-32, 34-37 and 43-47 depend from amended claims 1 and 30 and recite further limitations in combination with the novel elements of claims 1 and 30. Therefore, the allowance of claims 2-3, 5-8, 10, 14, 21-28, 31-32, 34-37 and 43-47 is also respectfully requested.

5.) Claim Rejections – 35 U.S.C. § 103(a)

The Examiner rejected claims 9, 12, 15, 17 and 38 under 35 U.S.C. § 103(a) as being unpatentable over Spear in view of Grimsrud, et al. (US 5,890,205). The Applicant respectfully traverses this rejection.

Specifically, claim 1, for instance states:

> 1. A processor system comprising:
> a processor,
> a first memory, *being of a random access memory type*,

a second memory, *being of a random access memory type*,

memory allocation means for allocation of data of a load module of said second memory to said first memory, said load module comprising:

variable/record data and/or instruction data,

an execution profiling section for providing execution data concerning behavior of programs executed in the processor system, continuously or intermittently, *whereby the operation of said means for memory allocation is software run-time updated based on said execution data*, said execution profiling section in turn comprising at least one means for measuring the performance characteristics of parts of said load module,

whereby said memory allocation means is arranged for allocation of selected parts of said load module to said first memory.

As noted above, Spear does not teach all of the elements of claim 1. Furthermore, Grimsrud does not make up for the elements missing from Spear. Thus, the combination of Spear and Grimsrud do not teach all of the elements of claims 1 or 30, nor of claims 9, 12, 15, 17 and 38.

As discussed above, the amended base claims 1 and 30 contain elements which are not found in Spear. As provided in MPEP § 2143, "[t]o establish a prima facie case of obviousness, ... the prior art reference (or references when combined) *must teach or suggest all the claim limitations*." Furthermore, under MPEP § 2142, "[i]f the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness." It is submitted that the Grimsrud patent does not provide the missing claim limitations. Thus, the combination of Spear and Grimsrud do not teach all of the claim elements. Consequently, the Office Action does not factually support a prima facie case of obviousness. The Applicant, therefore, respectfully requests that this rejection be withdrawn.

The Examiner rejected claims 11, 13 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Spear in view of Berry, et al. (US 6,662,358). The Applicant respectfully traverses this rejection.

Spear does not teach all of the elements of claim 1. Furthermore, Berry does not make up for the elements missing from Spear. Thus, the combination of Spear and Berry do not teach all of the elements of claim 1, nor of claims 11, 13, and 16.

As discussed above, the base claims 1 and 30 contain elements which are not found in Spear. As provided in MPEP § 2143, "[t]o establish a prima facie case of obviousness, ... the prior art reference (or references when combined) *must teach or suggest all the claim limitations*." Furthermore, under MPEP § 2142, "[i]f the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness." It is submitted that the Berry patent does not provide the missing claim limitations. Thus, the combination of Spear and Berry do not teach all of the claim elements. Consequently, the Office Action does not factually support a prima facie case of obviousness. The Applicant, therefore, respectfully requests that this rejection be withdrawn.

The Examiner rejected claims 18-20, 40 and 41 under 35 U.S.C. § 103(a) as being unpatentable over Spear in view of Zucker (US 5,991,871). The Applicant respectfully traverses this rejection.

Spear does not teach all of the elements of claims 1 or 30. Furthermore, Zucker does not make up for the elements missing from Spear. Thus, the combination of Spear and Zucker do not teach all of the elements of claims 1 or 30, nor of claims 18-20, 40 and 41.

As discussed above, the amended base claims 1 and 30 contain elements which are not found in Spear. As provided in MPEP § 2143, "[t]o establish a prima facie case of obviousness, ... the prior art reference (or references when combined) *must teach or suggest all the claim limitations*." Furthermore, under MPEP § 2142, "[i]f the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness." It is submitted that the Zucker patent does not provide the missing claim limitations. Thus, the combination of Spear and Zucker Do not teach all of the claim elements. Consequently, the Office Action does not factually support a prima facie case of obviousness. The Applicant, therefore, respectfully requests that this rejection be withdrawn.

Attorney Docket No. P12368

CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for all pending claims.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,

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